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OFDM MODULATOR/DEMODULATOR AND METHOD FOR SUPPORTING VARIABLE DATA RATE IN WIRELESS LAN SYSTEM

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Abstract

The present invention pertains to an OFDM modulator/demodulator and method applicable to an OFDM modem that can support a variable data rate. The present invention includes a MAC that generates a signal field and a data field constituting an OFDM frame structure according to an external control signal, or that receives a signal field and a data field; an OFDM modulation transmitter equipped with an OFDM modulation controller that receives the signal field and the data field from the above-mentioned MAC while exchanging a first prescribed control signal with the above-mentioned MAC and controls each block of an OFDM modulator based on the data rate and data length information included in the above-mentioned signal field so that a final OFDM symbol is generated by coupling with a preamble constituting the OFDM frame structure formed by extraction from a sequence value stored in advance; and an OFDM demodulator receiver equipped with an OFDM demodulation controller that transmits the signal field and the data field to the above-mentioned MAC while exchanging a second prescribed control signal with the above-mentioned MAC and controls each block of an OFDM demodulator based on the data rate and data length information included in the above-mentioned signal field so that an OFDM demodulation process is carried out. Therefore, this device is variable for all of the data rates prescribed in IEEE 802.11a/D7.0, and can be applied to a wireless LAN system that will require a high data rate in the future.

Representative figure:

Figure 1

Keywords:

OFDM modulation and OFDM demodulation

Specification

Brief description of the figures

Figure 1 is a constitutional diagram showing the OFDM modulation and demodulation system applied to the present invention.

Figure 2 is a constitutional diagram showing an OFDM frame structure of an application example of the present invention.

Figure 3 is a constitutional diagram showing a mixer of an application example of the present invention.

Figure 4 is a constitutional diagram showing a weaving encoder of an application example of the present invention.

Figure 5 is a constitutional diagram showing the synchronizer shown in Figure 1.

Figure 6 is a constitutional diagram showing the Viterbi decoder shown in Figure 1.

Figure 7 is a detailed diagram showing a memory and a TB of the Viterbi decoder shown in Figure 6.

Figure 8 is a detailed diagram showing a LIFO of the Viterbi decoder shown in Figure 6.

Detailed explanation of the invention

Purpose of the invention

Technical field of the invention and prior art of the field

The present invention pertains to OFDM (Orthogonal Frequency Division Multiplexing) modulation and demodulation that is suitable for a wireless LAN system and that supports a variable data rate. In particular, the present invention pertains to an OFDM modulator/demodulator and method applicable to an OFDM modem that can support all data rates from 6-54 Mbps based on the physical layer protocol of IEEE 802.a/D7.0.

In modulation and demodulation methods that are applied to wireless LAN systems, a FS [sic; FH] (Frequency Hopping) and SS (Spread Spectrum) method that can be realized in the 2.4 GHz band is well known. However, the OFDM modulation and demodulation method that can support a variable data rate has recently been studied.

In a wireless channel environment, an ISI (Intersymbol Interference) is generated by multipath propagation. For a single carrier, complicated equalizer hardware is required for a receiver to minimize ISI effects, whereas simple equalizer hardware is required to minimize ISI effects when modulation and demodulation are carried out by the OFDM method. Since a smaller bandwidth is required in OFDM because of utilization of the orthogonality between subcarriers, this modulation and demodulation method is suitable for a limited frequency band, and since frequency selective fading is converted into flat fading, the method is suitable for a wireless channel environment. In addition, since the modulation and demodulation of the OFDM method can vary the number of bits allocated to each subcarrier, it is suitable for high-speed data transmission.

In IEEE 802.11a as one of the standards for wireless LAN systems, data are transmitted and received in frame units, and a physical layer for the OFDM system is prescribed. In the above-mentioned IEEE 802.11a, a PLCP (Physical Layer Convergence Procedure) having information on data length, modulation method, transmission rate, etc., is added to a header part of data according to the characteristics of the LAN.

The present invention pertains to the OFDM modulation and demodulation method based on IEEE 802.11a/D7.0 that has recently been a focus of research and adopts the OFDM modulation and modulation method that supports a data rate of 6-54 Mbps at maximum in the 5 GHz band in IEEE 802.11a/D7.0.

The following Tables 1 and 2 show parameters that are used in the OFDM modulation and demodulation system prescribed in IEEE 802.11a/D7.0.

Table 1. Parameters according to data rates

데이터 속도 ①	맵핑 ②	부호율 ③	서브캐리어당 coded 비트수 ④	OFDM 심볼당 coded 비트수 ⑤	OFDM 심볼당 data 비트수 ⑥
6 Mbps	BPSK	1/2	1	48	24
9 Mbps	BPSK	3/4	1	48	36
12 Mbps	QPSK	1/2	2	96	48
18 Mbps	QPSK	3/4	2	96	72
24 Mbps	16QAM	1/2	4	192	96
36 Mbps	16QAM	3/4	4	192	144
48 Mbps	64QAM	1/2	6	288	192
54 Mbps	64QAM	3/4	6	288	216

Key: 1 Data rate
2 Mapping
3 Coding rate
4 Number of coded bits for each subcarrier (N_{EPSC})
5 Number of coded bits for each OFDM symbol (N_{CEPS})
6 Number of data bits for each OFDM symbol (N_{DBPS})

Table 2. Parameters related to time

① 파라미터	값 ②
N_{SD} : 데이터 서브캐리어 수	48
N_{SP} : 파일럿 서브캐리어 수	4
③ N_{ST} : 전체 서브캐리어 수	52(N_{SD} + N_{SP})
Δ F : 서브캐리어 주파수 간격	0.3125MHz(=20MHz/64)
T_{FFT} : IFFT/FFT 주기	3.2 μ s(1/Δ F)
$T_{PREAMBLE}$: 프리앰블 기간	16 μ s(T_{SHORT} + T_{LONG})
T_{SIGNAL} : 시그널 필드 기간	4.0 μ s(T_{GI} + T_{FFT})
T_{GI} : 보호구간 기간	0.8 μ s(T_{FFT}/4)
T_{GI2} : 프리앰블의 보호구간 기간	1.6 μ s(T_{FFT}/2)
T_{SYM} : 심볼 기간	4 μ s(T_{GI} + T_{FFT})
T_{SHORT} : 프리앰블의 short 심볼 기간	8 μ s(10*T_{FFT}/4)
T_{LONG} : 프리앰블의 long 심볼 기간	8 μ s(T_{GI2} + 2*T_{FFT})

Key: 1 Parameter
2 Value
3 N_{SD}: Number of data subcarriers
N_{SP}: Number of pilot subcarriers
N_{ST}: Total number of subcarriers
ΔF: Frequency spacing of subcarriers
T_{FFT}: IFFT/FFT period
$T_{PREAMBLE}$: Preamble period
T_{SIGNAL}: Signal field period
T_{GI}: Guard interval
T_{GI2}: Guard interval of preamble
T_{SYM}: Symbol period

T_{SHORT}: Short symbol period of preamble
T_{LONG}: Long symbol period of preamble

However, the known OFDM modulation and demodulation methods that meet IEEE 802.11a cannot perform modulation and demodulation according to the data rates of 6-54 Mbps by means of a single device.

Technical problems to be solved by the invention

The present invention has been proposed to solve the problems of the above-mentioned prior art, and the purpose of the present invention is to provide an OFDM modulator/demodulator and method that can support the variable data rates prescribed in IEEE 802.11a.

Constitution and operation of the invention

The OFDM modulator and demodulator capable of enabling MPDU transmission and reception at a variable data rate in a first configuration of the present invention is characterized by the fact that it includes a MAC that generates a signal field and a data field constituting an OFDM frame structure according to an external control signal, or that receives a signal field and a data field; an OFDM modulation transmitter equipped with an OFDM modulation controller that receives the signal field and the data field from the above-mentioned MAC while exchanging a first prescribed control signal with the above-mentioned MAC and controls each block of an OFDM modulator based on the data rate and data length information included in the above-mentioned signal field so that a final OFDM symbol is generated by coupling with a preamble constituting the OFDM frame structure formed by extraction from a sequence value stored in advance; and an OFDM demodulator receiver equipped with an OFDM demodulation controller that transmits the signal field and the data field to the above-mentioned MAC while exchanging a second prescribed control signal with the above-mentioned MAC and controls each block of an OFDM demodulator based on the data rate and data length information included in the above-mentioned signal field so that an OFDM demodulation process is carried out.

In addition, the data modulation method in the OFDM modulator and demodulator capable of enabling MPDU transmission and reception at a variable data rate in a second configuration of the present invention is characterized by the fact that it includes a first step that maps data to be transmitted based on data modulation and demodulation information and data transmission rate information included in a signal field of an OFDM signal received from a MAC; a second step that extracts a pre-stored preamble and generates a preamble consisting of several short symbols and long symbols; and a third step that allocates the above-mentioned

mapped data and a pilot signal to an IFFT-transformed subcarrier frequency and generates a final OFDM symbol by coupling the above-mentioned preamble.

On the other hand, the data demodulation method in an OFDM modulator and demodulator capable of enabling MPDU transmission and reception at a variable data rate of a third configuration of the present invention is characterized by the fact that it includes a first step that compensates the frequency offset of a received OFDM signal and generates a control signal for indicating the start of an OFDM symbol; a second step that FFT-transforms and equalizes the above-mentioned received OFDM signal and restores the original signal field through a Viterbi decoding process after demapping and deinterleaving based on the data rate information included in the above-mentioned signal field; and a third step that checks the parity of the restored signal field and transmits a signal field bit only if the parity is correct.

Other merits and characteristics of the present invention will be further clarified through the detailed explanation of the present invention. Next, an appropriate application example of the present invention will be explained in an illustrative manner, with reference to the attached figures.

As explained above, in the present invention, a method for controlling an OFDM transmission and reception part used to control an OFDM transmitter and receiver to support a variable data rate, a synchronization method for compensating the frequency offset of the OFDM transmitter and receiver, and a Viterbi decoder for correcting errors generated by a wireless channel are employed. The detailed explanation of the above-mentioned Viterbi decoder will be given later.

First, Figure 1 is an overall constitutional diagram showing an appropriate OFDM modulation and demodulation system of the present invention, and Figure 2 shows an example of an OFDM frame structure used in the present invention.

The OFDM frame structure shown in Figure 2 will be explained first, and Figure 1 will be explained as an example in detail.

The OFDM frame structure applied to the present invention, as shown in Figure 2, consists of preamble, a signal field, and a data field. The signal field and a service bit correspond to a PLCP header. As the input sequence for an IFFT (Inverse Fast Fourier Transform) (105) of the above-mentioned preamble, values stored in a ROM (107) are read out, and the input sequence consists of a short sequence (S-26, … 26) and a long sequence (L-26, … 26) as the following mathematical expression 1 given as an application example. When each sequence passes through the IFFT (105), it becomes a short symbol and a long symbol.

$S_{-26,\ldots,26}$ = sqrt(13/6)*{0,0,1+j,0,0,0,-1-j,0,0,0,1+j,0,0,0,
-1-j,0,0,0,-1-j,0,0,0,1+j,0,0,0,0,0,0,0,-1-j,0,0,0,
-1-j,0,0,0,1+j,0,0,0,1+j,0,0,0,1+j,0,0,0,1+j,0,0}

$L_{-26,\ldots,26}$ = {1,1,-1,-1,1,1,-1,1,-1,1,1,1,1,1,1,-1,-1,1,
1,-1,1,-1,1,1,1,1,0,1,-1,-1,1,1,-1,1,-1,1,-1,-1,-1,
-1,-1,1,1,-1,-1,1,-1,1,-1,1,1,1,1}

The above-mentioned mathematical expression 1 is an input sequence that is sequentially allocated to the -26th subcarrier frequency up to the 26th subcarrier frequency of the IFFT (105).

The preamble is used for the synchronization (201) of a receiver, and its structure consists of 10 short symbols (t) and 2 long symbols (T). A short symbol has 16 complex number values. In other words, t_1 to t_{10} respectively have 16 complex number values. A long symbol then has 64 complex number values. In other words, T_1 and T_2 respectively have 64 complex number values.

The signal field includes 4 bits showing a data rate transmitted from a MAC (40) and 12 bits showing the length of a data field. 4 bits showing the data rate are shown in Table 3 as an application example, and the data length is 4,095 bits at maximum.

Table 3. Bits showing data rates

데이터 속도 (1)	b0 b1 b2 b3 : 4비트 (2) (LSB MSB)
6 Mbps	1101
9 Mbps	1111
12 Mbps	0101
18 Mbps	0111
24 Mbps	1001
36 Mbps	1011
48 Mbps	0001
54 Mbps	0011

Key: 1 Data rate
2 4 bits

As shown in Figure 2, the MAC (40) constitutes a signal field of a total of 24 bits consisting of 4 bits showing the data rate, 12 bits showing the data length, 1 reserved bit, 1 parity bit, and 6 tail bits.

These 24 bits, as will be mentioned later, are directly input into a weaving encoder (102) without passing through a mixer (101). Since the constraint length of the weaving encoder (102) is 7 and the code rate is 1/2, the signal field output value from the weaving encoder is 48 bits. The output of the weaving encoder (102) is passed through an interleaver (103), subjected to a BPSK (Binary Phase Shift Keying) mapping (104), passed through the IFFT (105), and sent to a RF (Wireless Frequency) [transmitter] (30).

The data field is shown next in Figure 2, and the MAC (40) generates the data field so that a data field structure of service field, MPDU (MAC Protocol Data Unit), tail field, and pad bits is included. The above-mentioned service field has 16 items with values of '0' and the tail field has 6 items with values of '0'. For the pad bits, zeros are inserted so that the total number of bits, consisting of the service bits, the MPDU (MAC Protocol Data Unit), and the tail bits, is an integer multiple of N_{CBPS} (the number of coded bits for each OFDM symbol), and its calculation equations comprise mathematical expression 2.

N_{SYM} = ceiling ((16 + 8 * data length + 6)/N_{DBPS})

$N_{DATA} = N_{SYM} * N_{DBPS}$

$N_{PAD} = N_{DATA} - (16 + 8 * \text{data length} + 6)$

In the above mathematical expression 1, the ceiling ( ) function is a function that obtains the smallest integer value among the values in the parentheses. N_{SYM} is the number of OFDM symbols, N_{DATA} is the number of bits of the data field, and N_{PAD} is the number of pad bits.

The data field output from the MAC (40) is transmitted to the mixer (101). The data passed through the mixer (101) is passed through the weaving encoder (102), interleaved (103), and mapped (104) to BPSK, QPSK (Quadrature Phase Shift Keying), 16 QAM (Quadrature Amplitude Modulation), and 64 QAM according to the data rate of the signal field. The data mapped in this manner is passed through the IFFT (105) and sent to the RF (30).

Next, OFDM modulation and demodulation transmitter (10) of Figure 1, which is an overall constitutional diagram for the OFDM modulation and demodulation, will be explained.

The mixer (101) of Figure 1 has the same structure as shown in Figure 3, and is used to prevent the data received from the MAC from having the same continuous value. The polynomial expression for generation is mathematical expression 3, as an application example.

$S(X) = X^7 + X^4 + 1$

The mixed data is passed through the weaving mixer (102), which has the same structure as shown in Figure 4. The polynomial expression for generation is mathematical expression 4, as an application example.

LSB = 133_8

MSB = 171_8

Said LSB is the abbreviation for 'Least Signification Bit,' and MSB is the abbreviation for 'Most Significant Bit.'

The interleaver (103) is used to change a burst error, which is generated by a channel, to a random error. The interleaver (103) is passed through a two-stage substitution. The data passed through the weaving encoder (102) and the substitutions of the interleaver (103) are represented by mathematical expression (5), as an application example.

First substitution:

$$i = (N_{CBPS}/16) * (k \bmod 16) + \text{floor}(k/16)$$

Second substitution:

$$j = s * \text{floor}(i/s) + ((i + N_{CBPS} - \text{floor}(16 * i/N_{CBPS})) \bmod s)$$

$$s = \max(N_{BPSC}/2, 1)$$

In the above-mentioned mathematical expression 5, the floor ( ) function is a function for obtaining the largest integer value that does not exceed the value in the parentheses, k is an index of [data] passage through the weaving encoder (102), i is an index of passage through the first substitution, and j is an index of passage through the second substitution. In the above-mentioned mathematical expression 5, BPSK and QPSK are subjected to only the first substitution, and 16 QAM and 64 QAM are subjected to both the first substitution and the second substitution.

The data passed through the interleaver (103) is mapped by mapper (104), as shown in the following Tables 4, 5, 6, and 7, according to the data rate, the data mapped is divided into an in-phase component and a quadrature component, the mapped data is multiplied by a standardization vector for standardizing the power being transmitted, and the values are shown in Table 8 as an application example. The following Tables 4-8 respectively show an application example of the BPSK mapping, an application example of the QPSK mapping, an application example of the 16 QAM mapping, an application example of the 64 QAM mapping, and an application example of the standardization vector (K_{MOD}) according to the mapping.

Table 4

입력 비트 b0 (1)	위상성분 성분 (2)	직교성분 성분 (3)
0	-1	0
1	1	0

Key: 1 Input bit b0
2 In-phase component
3 Quadrature component

Table 5

입력 비트 b0 (1)	위상성분 성분 (2)	입력 비트 b1 (3)	직교성분 성분 (4)
0	-1	0	-1
1	1	1	1

Key: 1 Input bit b0
2 In-phase component
3 Input bit b1
4 Quadrature component

Table 6

입력 비트 b0b1 (1)	인페이즈 성분 (2)	입력 비트 b2b3 (3)	쿼드러처 성분 (4)
00	-3	00	-3
01	-1	01	-1
11	1	11	1
10	3	10	3

Key: 1 Input bit b0b1
2 In-phase component
3 Input bit b2b3
4 Quadrature component

Table 7

입력 비트 b0b1b2 (1)	인페이즈 성분 (2)	입력 비트 b3b4b5 (3)	쿼드러처 성분 (4)
000	-7	000	-7
001	-5	001	-5
011	-3	011	-3
010	-1	010	-1
110	1	110	1
111	3	111	3
101	5	101	5
100	7	100	7

Key: 1 Input bit b0b1b2
2 In-phase component
3 Input bit b3b4b5
4 Quadrature component

Table 8

매핑 (1)	K_{MOD}
BPSK	1
QPSK	1/sqrt(2)
16QAM	1/sqrt(10)
64QAM	1/sqrt(42)

Key: 1 Mapping

The data mapped in this manner is allocated to 48 subcarrier frequencies of the IFFT (105), and the pilot signal is allocated to the 7^{th}, 21^{st}, -7^{th}, and -21^{st} subcarrier frequencies of the IFFT (105). The data passed through the IFFT (105) appears as 64 in-phase components and quadrature components. Among the 64 values, the last 16 values are copied and put in front of the data passed through the IFFT to insert a guard interval (106). Therefore, one OFDM symbol is 4 μs and has 80 sample values.

In general, PCLP exists among the MAC (40), mixer (101), and inverse mixer (207), and in the present invention, the MAC (40) and OFDM modulation and demodulation controllers (1) and (2) divide and process the PLCP functions. In other words, the OFDM modulation and demodulation controllers (1) and (2) control each function required for data transmission and reception, and the MAC (40) generates a signal field and a data field as shown in Figure 2.

The MAC (40) sends a control signal (tx_start) for the data transmission to the OFDM modulation controller (1) before sending the signal field and data field to an OFDM modulation transmitter (60). If a tx_start signal is received, first the OFDM modulation controller sends the short sequence value and long sequence value in the ROM (107) to the IFFT (105) to create the preamble of Figure 2, and generates a preamble.

If the short sequence value and the long sequence value are transmitted to the IFFT (105), a control signal (tx_ready) for receiving data of the signal field and data field is transmitted to the MAC (40). The tx_ready signal has values of '1' and '0,' and while the value is '1,' the MAC (40) sends bits of the signal field and the data field to the OFDM modulation controller (1). Since the signal field has 24 bits, the OFDM modulation controller (1) generates the signal field so that tx_ready has a value of '1' for only 24 bits and generates the data field data so that tx_ready has a value of '1' for only the number of data bits (N_{DBPS}) for each OFDM symbol according to the data rate of the signal field.

Since the first 24 bits are the signal field, the above-mentioned OFDM modulation controller (1) immediately transmits the bits to the weaving encoder (102), and since the bits after the signal field belong to the data field, the controller transmits the bits to the mixer (101). In addition, 4 bits for the data rate of the signal field are provided to the interleaver (103) and mapper (104) so that the OFDM modulation transmitter (60) can be operated according to the variable data rate.

Next, the structure of an OFDM demodulation receiver (70) will be explained.

In a received OFDM signal, an error of +/- 20 ppm is generated due to an independent RF oscillator, and appears as a frequency offset. The frequency offset is therefore generated in the received OFDM signal, and this frequency offset must be compensated. In the present invention, the synchronizer (201) of the OFDM demodulator (20), as shown in Figure 5, has a structure (50) for obtaining OFDM symbol synchronization, a structure (51) for roughly compensating the frequency offset, and a structure (52) for precisely compensating the frequency offset.

The values of a matched filter (501) are conjugate complex number values of 16 short symbols. The received OFDM signal is multiplied by the values of the matched filter (501), and their absolute values are adopted. In this case, the largest value is generated for every 16 short symbols. A highest value detector (502) detects these values and sends them to an OFDM symbol synchronization control (503). Since one OFDM symbol has 80 complex number values,

the OFDM symbol synchronization control (503) controls a counter being incremented from 1 up to 80, referring to the highest values that are generated for every 16 symbols, and sends a signal (rx_start) showing the start of the OFDM symbol to the OFDM demodulation controller (2).

A frequency offset estimator (511) estimates the frequency offset by utilizing two short symbols (t6, t7) of the preamble. A frequency offset average calculator (512) averages the estimated frequency offsets and sends the frequency offset average value to an NCO (Numerically Controlled Oscillator) (513). The NCO (513) obtains a sine value and a cosine value corresponding to the frequency offset average value. The received OFDM signal is multiplied by the sine value and cosine value obtained in this manner enable rough compensation of the frequency offset. A precise frequency offset is obtained from the frequency offset roughly compensated in this manner by utilizing two short symbols (t9, t10) through a frequency offset estimator (521). A frequency offset average calculator (522) averages the precise frequency offsets and sends the frequency average value to an NCO (523). The frequency offset is therefore compensated for the short symbols of the preamble, and the reason for this is that an equalizer (203) can make a precise channel estimation by means of a channel estimator utilizing long symbols of the preamble only when the frequency offset must be compensated prior to the long symbols.

From the data for which the frequency offset has been compensated in this manner, the guard interval is removed in the FFT (511), and the data is passed through an FFT. The data passed through the FFT is input to the equalizer (203). The equalizer (203) estimates channels corresponding to the frequency of each subcarrier. The channel values estimated in this manner are multiplied with an equalizer input signal to compensate the channels. The data passed through the equalizer (203) is passed through a demapper (204). The demapped data is passed through a deinterleaver (205), and the deinterleaver (205) carries out two substitutions. One application example of this is shown by mathematical expression 6.

First substitution:

$$i = s * \mathrm{floor}(j/s) + ((j + \mathrm{floor}(16 * j/N_{CBPS}))\bmod s)$$

$$s = \max(N_{BPSC}/2, 1)$$

Second substitution:

$$k = 16 * i - (N_{CBPS} - 1) * (\mathrm{floor}(16 * i/N_{CBPS}))$$

Here, j is an index of data passage through the demapper (204), i is an index of passage through the first substitution, and k is an index of passage through the second substitution. The data passed through the deinterleaver (205) is input into a decoder (206).

The Viterbi decoder (206) detects and corrects errors in the channels and consists of BM (Branch Metric) part (602), ACS (Add Compare Select) part (603), TB (Trace Back) part (605), memory (604), LIFO (Last In First Out) part (606), and control part (601). In the present

invention, the weaving encoder (102) with a constraint length of 7 and a code rate of 1/2 was decoded, hard decisions were made by means of Hamming distance, and the truncation length (decoding depth) was set to 48.

The BM part (602) calculates distance values between an input symbol and code words in each state, carries out a BM process for data being input from the deinterleaver (205) according to signal field and data field sections, and transmits the calculated BM value to the ACS part (603).

The ACS part (603) updates a new path value by the distance value transmitted from the above-mentioned BM part (602) and the accumulated path values up to the previous state, selects one of two paths being input at an optional time, and stores information on a survival path in the memory (604). Similarly to the BM part (602), the ACS part (603) divides the data into signal field and data field sections and carries out a calculation process. The reason for this is that the data of the signal field and the data of the data field can have different demodulation rates.

Memory (604) implements functions of storing information on the survival path selected by the above-mentioned ACS part (603) and transmitting data to the TB part (605) to trace back the data. In the above-mentioned TB part (605), a 3-pointer algorithm is applied using 6 memory banks to process high-speed data. Each memory has 24 addresses which are half of the truncation length (decoding depth), and has a length of 64 bits for each address. Therefore, the data being input are divided into 24 address units and repeatedly read from and written into each memory bank. This has a thread of connection with the constitution of the signal field and data field data of multiples of 24.

The TB part (605) carries out a trace-back by using the information on the survival path stored in the above-mentioned memory (604). For the signal field and the data field, data decoding in the TB part (605) is advanced by slightly different methods. At the time of transmission, information showing the modulation and demodulation methods and as information showing the length of data being transmitted can be detected at the same time as the input of the signal field, but at a reception terminal the information can be detected only after decoding the signal field in the Viterbi decoder (206). Therefore, at the time of reception the information showing the modulation and demodulation methods should be transmitted to the demapper (204) and the deinterleaver (205) from the Viterbi decoder (206), but at that time a time delay (latency) due to the trace-back is generated in the Viterbi decoder (206).

In the present invention, however, since there are 6 tail bits at the end of the signal field being transmitted, the signal field is immediately decoded from the '00000' state without tracing back the continuous data field in order to reduce the latency of the signal field. Once the information showing the modulation and demodulation methods and the information about the length of the data being transmitted are detected by means of the signal field, the data field starts

their trace-back and decoding by a demodulation method appropriate to the information showing the modulation and demodulation methods. Since the 3-pointer algorithm has been applied for trace-back, 3 modules (702) for trace-back are used in the TB part (605). In an alternating fashion, two of the above-mentioned three trace-back modules (702) carry out the trace-back, and one module carries out the decoding process. As mentioned above, one module among three trace-back modules (702) is in charge of decoding and is selected by a control signal (dec_read_pointer). The data decoded by the TB part (605) have an arrangement structure in which the order is reversed. The reason for this is that when the data are read out of memory (701) to implement the trace-back, the data are read out in reverse order. Therefore, the LIFO part (606) is used to rearrange the data into the original order. The above-mentioned LIFO part (606) performs reading and writing in an alternating fashion by using two memories. Using a control signal (Ram_switch) (801), when the above-mentioned control signal (801) is '0,' a first memory (802) carries out writing, and a second memory (803) carries out reading. Conversely, when the above-mentioned control signal (801) is '1,' the first memory (802) carries out reading, and the second memory (803) carries out writing. If decoding of all the received data field data is finished, the Viterbi decoder (206) transmits a decoding completion signal to the demodulation controller (2) and sets each function block of the reception part to have an initial value. This setting can be obtained by comparing the information on the data transmission length in the signal field with the length information counted in the Viterbi decoder (206).

The data passed through the decoder (206) are passed through an inverse mixer (207). An application example of the polynomial expression for the generation of the inverse mixer (207) is shown by the expression (2). The initial 7 bits being input into the inverse mixer (207) are used as values for initializing said inverse mixer.

The OFDM demodulation controller (2) for controlling the OFDM demodulator (20) receives the signal (rx_start) showing the start of the OFDM symbol from the synchronizer (201) and informs the FFT (202) of the signal. The FFT (202) receives the rx_start signal, keeps the remainder of 64 samples excepting the 16 sample values of the guard interval, and carries out the FFT (202). In Figure 2, the signal field including the data rate and the data length of the OFDM frame being transmitted is first passed through the FFT (202) and the equalizer (203).

Since the signal field is modulated by the BPSK method, the demapper (204) and the deinterleaver (205) at the reception terminal are operated according to the BPSK method. The signal field passed through the deinterleaver (205) is input into the Viterbi decoder (206). Since the Viterbi decoder (206) carries out a process for decoding the data which was decoded by the weaving decoder to restore the original data, the transmitted original signal field can be restored only after the received signal field passes through the Viterbi decoder (206).

Since the signal field passed through the Viterbi decoder (206) is not mixed, it is input into the OFDM demodulation controller (2) without passing through the inverse mixer (207). The OFDM demodulation controller (2) checks the parity of the signal field and sends the bits of the signal field to the MAC (40) if the parity is correct. At that time, since the signal field is 24 bits, a signal (rx_ready) of '1' is generated for 24 bits, and the bits of the signal field are transmitted. The MAC (40) receives the bits from the OFDM demodulation receiver (70) only while rx_ready is '1.'

In addition, the OFDM demodulation controller (2) stores 4 bits showing the data rate of the signal field and 12 bits showing the data length. The OFDM demodulation controller (2) informs the demapper (204) and the deinterleaver (205), which are operated according to the data rate, of the 4-bit information indicating the data rate so that the OFDM demodulator (20) can be operated according to the variable data rate. The OFDM demodulation controller (2) then calculates the number of OFDM symbols corresponding to 12 bits indicating the data length, and stops the operation of the OFDM demodulator (20) when the number of OFDM symbols calculated is equal to the number of OFDM symbols received.

In Figure 2, the data field appears after the signal field, and the data field is also passed through the FFT (202), equalizer (203), demapper (204), deinterleaver (205), Viterbi decoder (206), and inverse mixer (207). The bits of the inversely mixed data field are input to the OFDM demodulation controller (2), and the OFDM demodulation controller (2) generates rx_ready so that it has a value of '1' for only the number of data bits (N_{DBPS}) for each OFDM symbol according to the data rate. The OFDM demodulation controller (2) transmits the rx_ready signal and the bits of the data field to MAC (40), and MAC (40) receives the bits from the OFDM demodulation controller (2) only while the rx_ready signal is '1.'

Effects of the invention

According to the OFDM demodulation and modulation methods of the present invention, modulation and demodulation are constituted by OFDM methods that are suitable for a wireless LAN system and permit variability for all the data rates prescribed in IEEE 802.11a/D7.0. Therefore, these methods can be applied to wireless LAN systems that will require high-speed data in the future.

The explanation up to this point shows an application example appropriate for understanding the present invention, but the present invention is not limited to this. It is evident to any person with ordinary knowledge in this technical field that the present invention can be variously modified and changed without departing from the scope of the patent claims and their gist.

Claims

1. An OFDM modulator and demodulator, characterized by the fact that in an OFDM modulator and demodulator capable of enabling MPDU transmission and reception at a variable data rate, it includes a MAC that generates a signal field and a data field constituting an OFDM frame structure according to an external control signal, or that receives a signal field and a data field; an OFDM modulation transmitter equipped with an OFDM modulation controller that receives the signal field and the data field from the above-mentioned MAC while exchanging a first prescribed control signal with the above-mentioned MAC and controls each block of an OFDM modulator based on the data rate and data length information included in the above-mentioned signal field so that a final OFDM symbol is generated by coupling with a preamble constituting the OFDM frame structure formed by extraction from a sequence value stored in advance; and an OFDM demodulator receiver equipped with an OFDM demodulation controller that transmits the signal field and the data field to the above-mentioned MAC while exchanging a second prescribed control signal with the above-mentioned MAC and controls each block of an OFDM demodulator based on the data rate and data length information included in the above-mentioned signal field so that an OFDM demodulation process is carried out.

2. The OFDM modulator and demodulator of Claim 1, characterized by the fact that the above-mentioned OFDM modulation controller separately processes the bits of the above-mentioned signal field and data field, respectively, and transmits a detected data rate to a mapper and an interleaver to implement appropriate mapping and interleaving according to the data rate.

3. The OFDM modulator and demodulator of Claim 1, characterized by the fact that the above-mentioned OFDM demodulation controller transmits information about the modulation and demodulation methods, extracted from the signal field of a received OFDM signal obtained from a Viterbi decoder among the blocks of the above-mentioned OFDM demodulator, and information about the length of data being transmitted to a demapper and a deinterleaver, calculates the number of OFDM symbols from the bits showing the data length of the signal field, compares it with the number of OFDM symbols received, and stops the operation of the OFDM demodulator when these two numbers of symbols are equal.

4. The OFDM modulator and demodulator of Claim 3, characterized by the fact that the above-mentioned Viterbi decoder transmits the data rate and data length information for the data being transmitted from the OFDM demodulator by using a 3-pointer algorithm without a trace-back latency.

5. The OFDM modulator and demodulator of Claim 1, characterized by the fact that the above-mentioned OFDM demodulation receiver includes a synchronizer for compensating the frequency offset of the received OFDM signal; and the above-mentioned synchronizer is equipped with a first compensator that estimates frequency offsets by utilizing two short symbols

of the preamble of the received OFDM signal, obtains an average value of the estimated frequency offsets, and obtains a sine value and a cosine value of the average value, a second compensator that estimates frequency offsets of the signal by utilizing two short symbols wherein the output of the above-mentioned first compensator and the received OFDM signal are multiplied and the frequency offset is roughly compensated, obtains an average value of the estimated frequency offsets, and obtains a sine value and a cosine value of the average value, and a synchronism acquirer that detects the highest value being generated for each short symbol by multiplying the signal by a matched filter with conjugate complex number values of the short symbols of the preamble of the received OFDM signal, and generates a control signal showing the start of the OFDM symbol.

6. A modulation method, characterized by the fact that in a data modulation method in an OFDM modulator and demodulator capable of enabling MPDU transmission and reception at a variable data rate, it includes a first step that maps data to be transmitted based on data modulation and demodulation information and data transmission speed information included in a signal field of an OFDM signal received from a MAC; a second step that extracts a pre-stored preamble and generates a preamble consisting of several short symbols and long symbols; and a third step that allocates the above-mentioned mapped data and a pilot signal to an IFFT-transformed subcarrier frequency and generates a final OFDM symbol by coupling the above-mentioned preamble.

7. The modulation method of Claim 6, characterized by the fact that the above-mentioned first step consists of a fourth step that divides the received OFDM signal into a data field and a signal field and generates the LSB and the MSB by mixing and weaving-encoding the data field; a fifth step that substitutes the data obtained in the above-mentioned fourth step through an interleaving processing of one or more substitution steps; and a sixth step that maps the above-mentioned substituted data based on the data rate information included in the above-mentioned signal field.

8. A demodulation method, characterized by the fact that in a data demodulation method in an OFDM modulator and demodulator capable of enabling MPDU transmission and reception at a variable data rate, it includes a first step that compensates the frequency offset of a received OFDM signal and generates a control signal for indicating the start of an OFDM symbol; a second step that FFT-transforms and equalizes the above-mentioned received OFDM signal and restores the original signal field through a Viterbi decoding process after demapping and deinterleaving based on the data rate information included in the above-mentioned signal field; and a third step that checks the parity of the restored signal field and transmits signal field bits to a MAC only if the parity is correct.

9. The demodulation method of Claim 8, characterized by the fact that it further includes a fourth step that calculates the number of OFDM symbols corresponding to the bits showing the data length included in the above-mentioned signal field, and stops OFDM demodulation operation when the number of OFDM symbols calculated is equal to the number of OFDM symbol received.

10. The demodulation method of Claim 8, characterized by the fact that the above-mentioned first step consists of a first compensation step that estimates frequency offsets by utilizing two short symbols of the preamble of the received OFDM signal, obtains an average value of the estimated frequency offsets, and obtains a sine value and a cosine value corresponding to the average value; a second compensation step that estimates frequency offsets of the signal wherein the signal compensated by means of the first compensation step and the above-mentioned received OFDM signal are multiplied by utilizing two other short symbols, obtains an average value of the estimated frequency offsets, and obtains a sine value and a cosine value corresponding to the average value; and a synchronism acquisition step that obtains the highest value for each short symbol by using a matched filter with a conjugate complex number value of one short symbol and generates the above-mentioned control signal by utilizing the highest value.

11. The demodulation method of Claim 8, characterized by the fact that the above-mentioned Viterbi decoding processing employs a 3-pointer algorithm using 6 memory banks for a high-speed data processing; and if decoding of the received data is finished, a decoding end signal for stopping the decoding procedure is generated.

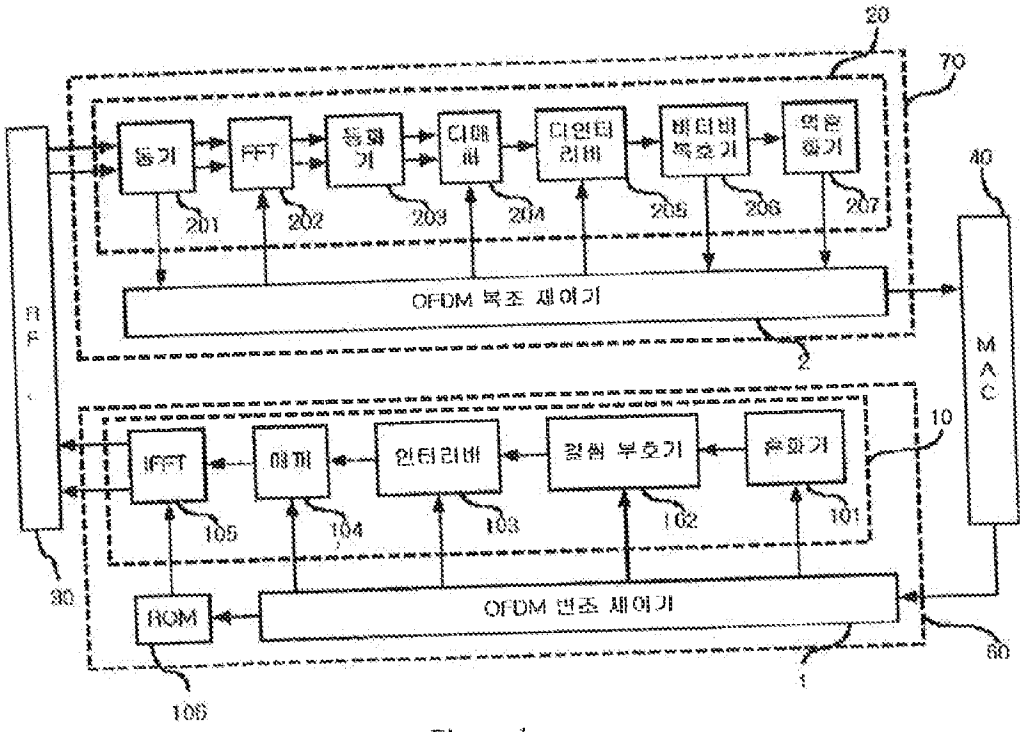

Figure 1

Key:
1 OFDM modulation controller
2 OFDM demodulation controller
101 Mixer
102 Weaving encoder
103 Interleaver
104 Mapper
201 Synchronizer
203 Equalizer
204 Demapper
205 Deinterleaver
206 Viterbi decoder
207 Inverse mixer

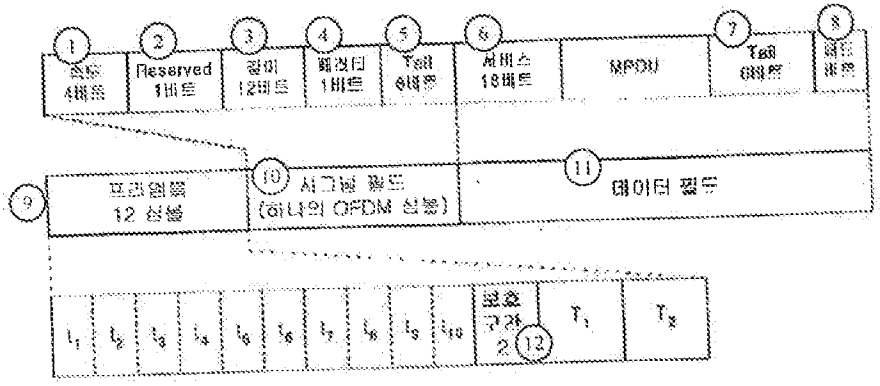

Figure 2

Key: 1 Rate - 4 bits
2 Reserved - 1 bit
3 Length - 12 bits
4 Parity - 1 bit
5 Tail - 6 bits
6 Service - 16 bits
7 Tail - 6 bits
8 Pad bits
9 Preamble - 12 symbols
10 Signal field (one OFDM symbol)
11 Data field
12 Guard interval 2

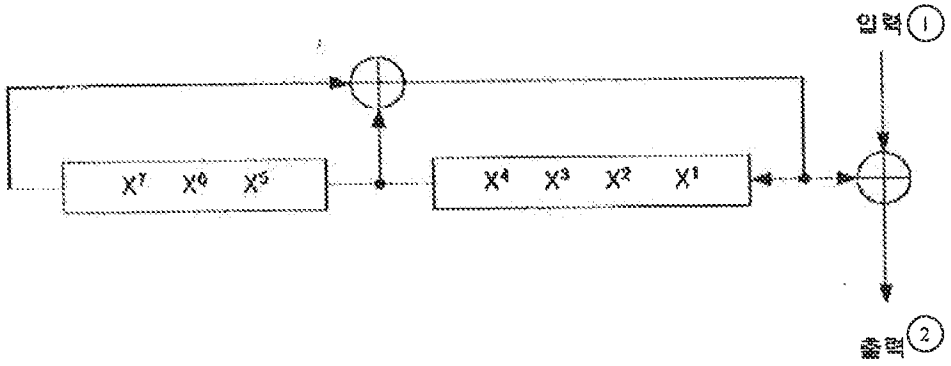

Figure 3

Key: 1 Input
2 Output

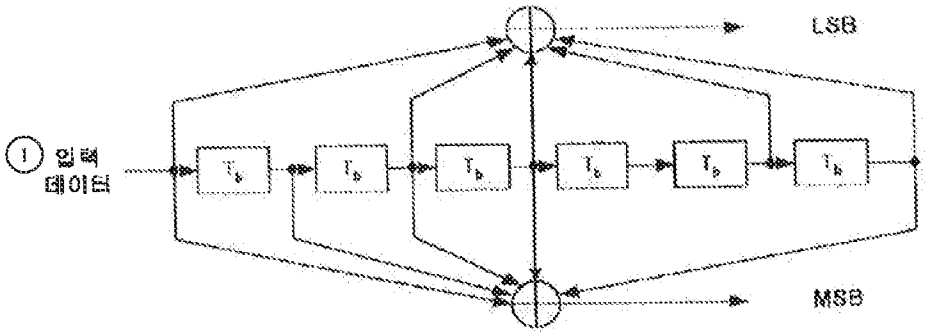

Figure 4

Key: 1 Input data

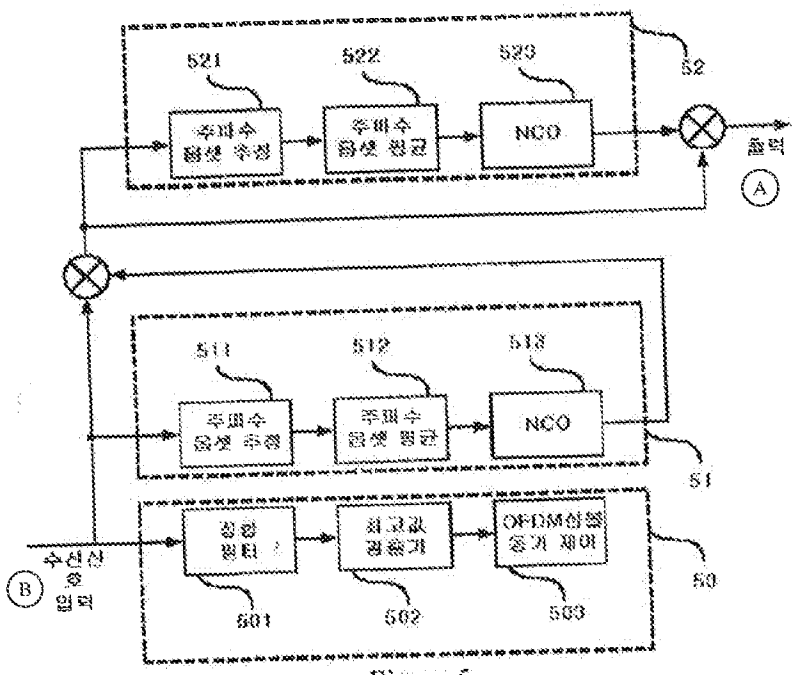

Figure 5

Key:
- A Output
- B Received signal input
- 501 Matched filter
- 502 Highest value detector
- 503 OFDM symbol synchronization control
- 511 Frequency offset estimation
- 512 Frequency offset average
- 521 Frequency offset estimation
- 522 Frequency offset average

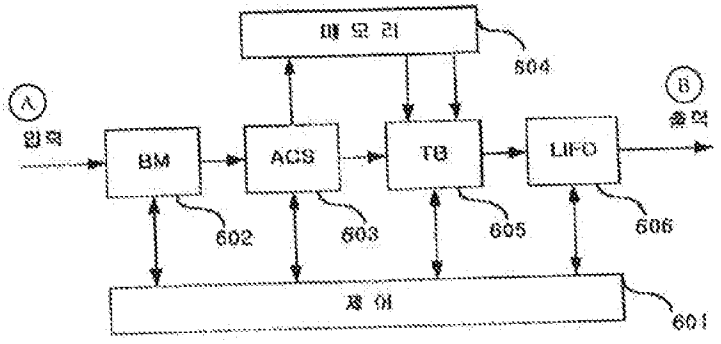

Figure 6

Key:
- A Input
- B Output
- 601 Control
- 604 Memory

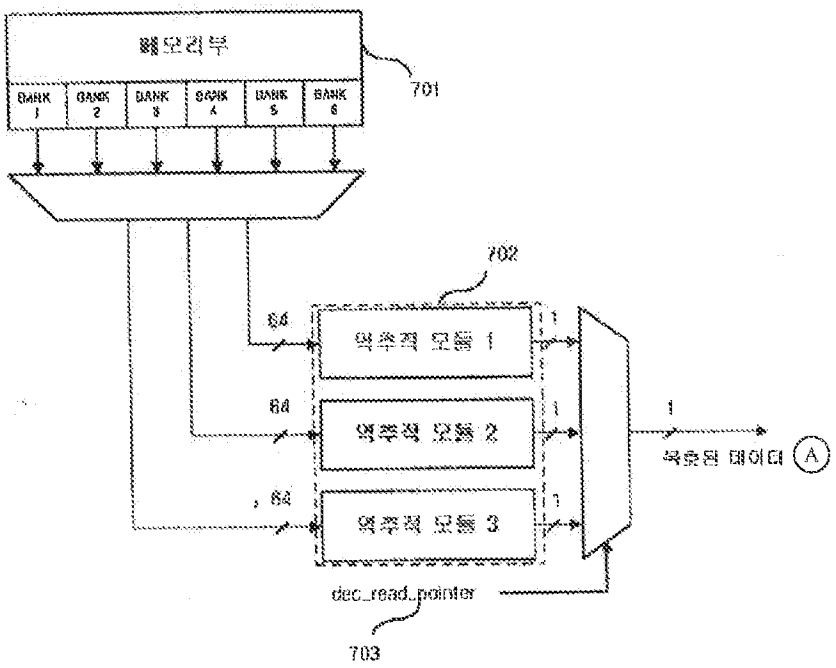

Figure 7

Key: A Decoded data
701 Memory
702 Trace-back module 1
Trace-back module 2
Trace-back module 3

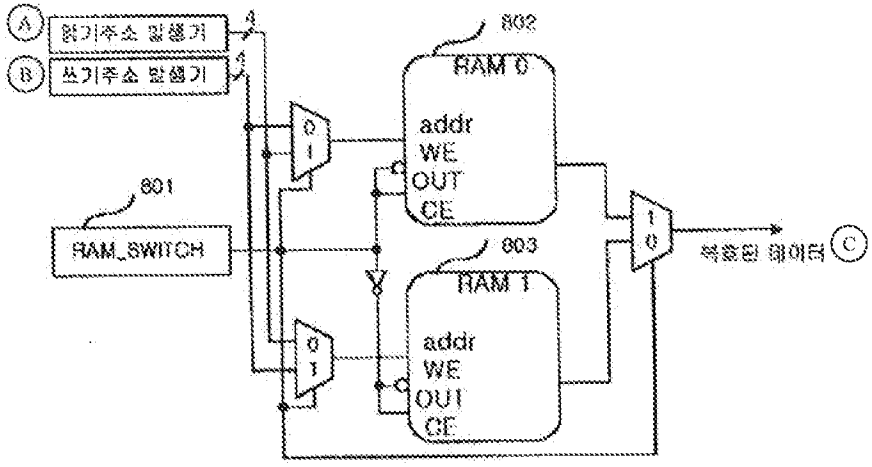

Figure 8

Key: A Read address generator
B Write address generator
C Decoded data